REMARKS

Claims 1-2 and 4-7 were rejected as unpatentable over YASUI et al. 5,248,963 in view of KANEDA JP 11271715. Reconsideration and withdrawal of the rejection are respectfully requested.

The Official Action does not provide a translation of KANEDA, but provides a summary of what is alleged to be disclosed in the reference. Since no translation has been made available, the accuracy of the allegation in the Official Action cannot be evaluated. An English abstract (copy in the Appendix) of the reference and the characterizations of KANEDA in the translations of Japanese and Korean official actions (provided in IDS's) do not support the characterization of the reference in the Official Action. For example, the abstract and IDS's do not mention detecting an absence of a sync signal and outputting a same potential to a common electrode and data lines, as is alleged in the Official Action. The Examiner is hereby requested to provide a translation of the reference so that the basis for the allegations in the Official Action can be properly evaluated. The Board of Patent Appeals and Interferences has stated in a non-precedential opinion (*Ex parte Jones*, 62 USPQ2d, 1206, BPAI, 2001), "In the event a reference is in a foreign language, if the applicant does not wish to expend resources to obtain a translation, the applicant may wish to request the examiner to

supply a translation. If the translation is not supplied by the examiner, the applicant may wish to consider seeking supervisory relief by way of a petition to have the examiner directed to obtain and supply a translation."

Claims 1 and 7 provide, among other features, that when at least one of the video signal, horizontal synchronization signal, and vertical synchronization signal is no longer being input to the liquid crystal display device, all the gate lines are activated and the common electrode potential is applied to the data lines. This will discharge the display capacitance and help prevent formation of an afterimage. The Official Action acknowledges that YASUI et al. do not disclose detecting the absence of video or sync signal.

YASUI et al. disclose a device (Figure 1) that includes a liquid crystal display panel 10 that receives inputs from gate bus drive circuit 17 and source bus drive circuit 16. The horizontal synchronization signal Hs and vertical synchronization signal Vs are input to gate bus drive circuit 17 and data (video) signal D is input to source bus drive circuit 16. Power for the device provided at V1. As shown in Figure 5, voltage drop detector 24 detects when power V1 is turned OFF. Voltage drop detector 24 is not associated with horizontal synchronization signal Hs and vertical synchronization signal Vs and does not detect when they are no longer being input. As is apparent,

these signals could still be input to the device even when the power is OFF (they may not be doing anything, but they are still being input.) YASUI et al. senses and responds to the power input, regardless of the status of the synchronization and video signal inputs.

As explained in the present application, one of the problems with the prior art was that in some devices the power is not turned OFF and thus there must be some other way of preventing an afterimage. Accordingly, the present invention senses and responds to the synchronization and video inputs specified in the claims, regardless of the power input, which is the opposite of YASUI et al.

The Official Action relies on KANEDA for the suggestion to modify the device in YASUI et al. so that when at least one of the video signal, horizontal synchronization signal, and vertical synchronization signal is no longer being input to the liquid crystal display device, all the gate lines are activated and the common electrode potential is applied to the data lines.

As noted above, the Official Action has not provided any evidence in support of the allegation that YASUI et al. teaches this limitation. Until such time as supporting evidence is provided, applicant denies that KANEDA provides the missing teaching and motivation. The English abstract and characterizations in the translations of the Japanese and Korean

official actions do not support the allegation in the Official Action. Reconsideration and withdrawal of the rejection are respectfully requested.

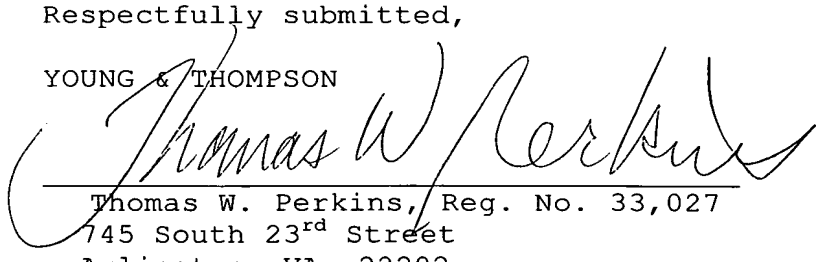
In addition, claims 1 and 7 have been amended to include the subject matter of claim 6 (support in Figure 1 and at page 15, lines 14-17). The drawings in KANEDA do not disclose that the predetermined time is determined based on a time constant of a resistor and a capacitor. Accordingly, claims 1 and 7 further avoid the combination of YASUI et al. and KANEDA and the amended claims are allowable over the art of record.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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